CLAIMS

What is claimed is:

1. An embedded dynamic random access memory (DRAM) comprising:

charge storage cells formed at intersections of word lines and complementary bit line pairs;

bit line sense amplifiers for fully sensing bit line data to full logic levels;

complementary data bus pairs for transferring said fully sensed bit line data from said bit line pairs, said data bus pairs running in a direction parallel to said bit line pairs; and

read and write amplifiers coupled to said data bus pairs for reading said fully sensed bit line data from said data bus pairs and writing buffered input data to said data bus pairs, respectively, with no Y-decoder.

2. An embedded memory as in claim 1 wherein said memory is embedded within an application specific integrated circuit (ASIC).

3. An embedded dynamic random access memory (DRAM) comprising:

charge storage cells formed at intersections of word lines and complementary bit line pairs, said bit line pairs running in a first direction on said memory;

bit line sense amplifiers for fully sensing bit line data to full logic levels;

complementary data bus pairs for transferring said fully sensed bit line data from said bit line pairs, said data bus pairs running in a direction parallel to said bit line pairs;

a plurality of data bus amplifiers for sensing selectable pages of data and transferring the data to cache registers.

4. An embedded memory as in claim 3 wherein said memory is embedded within an application specific integrated circuit (ASIC).